Dr. Rockstraw
CHME 391, Industrial Employment

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My name is Adam Michael Navarro and I was born and raised in Las Cruces, New Mexico. I chose to become a chemical engineer because I fancied chemistry as a high school student. Couple that with my skills in mathematics, and chemical engineering appeared to be the logical decision. The local chapter of the American Institute of Chemical Engineers (AIChE) would further push me in the direction of New Mexico State's chemical engineering program, as members of the chapter visited my advanced placement chemistry course at Oñate High School in the spring of 2011. It had been apparent to me that the students in AIChE had camaraderie amongst each other; this was a largely important factor in joining the chemical engineering program at NMSU. Despite the tales of countless hours spent in Jett Hall and the stories of late nights in Aspen, I enrolled at New Mexico State and chose chemical engineering as my major. It's been five years since, and I have completed CHME 307 thus far. This fall I will take CHME 452 and CHME 412, and intend on graduating with a B.S. in chemical engineering with minors in chemistry and materials engineering.

I have learned quite a bit at Intel this summer. This internship allowed me to gain knowledge on wet chemical benches and how they are used in the semiconductor fabrication process. First and foremost to this summer's experience has been maintaining and owning a silicon nitride (Si_3N_4) etching tool set. I learned about two different layers, PINT and SPCR, and how the wet chemical benches are used in each. I have gained a new perspective on the semiconductor manufacturing process and how various tools are used in order to construct Intel's products.

The tools I had ownership over are silicon nitride etches at two layers: PINT and SPCR. At PINT, a 100:1 H_2O: HF (hydrofluoric acid) solution is used to remove silicon dioxide (SiO_2) on top of a layer of silicon nitride. Then, isolation nitride is removed by hot ortho-phosphoric acid (H_3PO_4) at 160 degrees Celsius. The etch rate of silicon nitride is far greater than that of silicon dioxide; a typical selectivity is on the order of about 40:1. The SPCR operation involves a brief HF dip to remove any oxides; an oxide on the hard mask on top of the poly is removed, and the hard mask is removed by phosphoric acid.

I have learned about the Marangoni principle, which is seen on the low pressure dryer within the cleaning entities within the tool sets. Heated isopropyl alcohol (IPA) creates a meniscus at the wafer surface which forces water away in the water bath clean. Surface tension gradients in thin aqueous films cause films of water to flow off the wafer surface. The clean entities must operate in nitrogen vapor, where IPA percentage in water is less than one percent.

I have learned a bit about the devices Intel creates. In a handful a device physics courses, I learned about MOS capacitors, band diagrams, and the difference between p-type and n-type dopants. I also learned about and the overall flow of operations in which I was involved. In short, oxide and nitride are placed on a silicon wafer via diffusion, then resist is placed upon the oxide and nitride so that trenches can be etched. The wafer is then cleaned in a series of cleaning tools which do not affect the lithography. The trenches are then coated and filled with oxide. Once planarized, the nitride etch tools work on silicon nitride with the phosphoric acid, as mentioned above.

As a tool owner, I saw them firsthand in the factory, getting a better feel for how exactly they operate and what types of issues are commonplace. Intel as a company places safety as a high, if not the highest priority. I was around acids such as hydrofluoric and phosphoric, chemicals which require proper PPE. These included a shield, apron, and handling gloves. The technicians showed me how to properly don these items and how to be safe around chemicals and the machinery. Communication was key not only with the technicians (who have more experience with the tool set than myself) but also with more experienced engineers who have had to deal with my tool set in years past. I also communicated with quality engineering and integration in events in which we had to evaluate any potential impact to the silicon wafers. This communication was successful in that it allowed engineering to right any potential misprocessing, and deliver the best product possible before sent to final assembly in another Intel fab.

A second objective of my internship was to research what technologies are available for real time monitoring of chemical concentrations. I was able to utilize academic search engines such as the American Chemical Society (ACS) and Science Direct in order to determine what technologies were possible. In short, differential electrochemical mass spectrometry (DEMS) could be used in chemical baths to sample the concentrations of small, volatile compounds such as O_2, NH_3, and CO_2. This technology uses a set of electrodes in order to convert chemical energy into electrical signals. A mass voltammogram is then generated in order to identify the species in solution.

This internship has provided invaluable experience, as I have now have about twelve months' time with this company. Having owned a tool set was a large duty for a young engineer, but I feel that NMSU's chemical engineering program has provided me with both the technical and communication skills I need to be successful. As far as the research goes, I did find it unfortunate that I was only able to look into chemical monitoring technologies rather than construct an apparatus in order to do so, as well. This came out of the factory need to reduce costs; weekly silicon wafer startups were limited in numbers and my team's objectives were to simply ensure that we run a safe and reliable process, rather than find solutions to our defect modes. Still, the skills I acquired were important and will serve me well as I continue my career. It should be noted that my success at Intel has paved a path for success in any engineering career that I may choose due to my skills gained throughout this and prior internships.